Abstract of Disclose

A semiconductor device, for use in a semiconductor memory device, for controlling a core voltage generator for providing a core voltage to be coupled to a bit line sensing amplifier, comprises a bit line sensing start signal controller for receiving a bit line sensing start signal to generate a delayed bit line sensing start control signal in response to a refresh signal; a core overdriving controller for generating an overdriving control signal in response to the delayed bit line sensing start signal; and a core voltage generator for generating the core voltage in response to the delayed bit line sensing start signal and the overdriving control signal to thereby provide core voltage to the bit line sensing amplifier after a predetermined delayed time from the bit line sensing start control signal.